<u>CLAIMS</u>

What is claimed is:

1. A method of processing a predicated instruction comprising:

receiving a consumer instruction in an reservation station of an out-order processor;

receiving a predicated instruction in the reservation station, wherein the consumer instruction depends on a result of the predicated instruction;

dispatching the predicated instruction to an execution unit;

executing the predicated instruction; and

storing the executed predicate instruction in a re-order buffer.

2. The method of Claim 1, wherein dispatching the predicated instruction to an execution unit includes stalling the predicated instruction until all non-predicated dependencies are resolved.

3. The method of Claim 1, further comprising:

resolving the predicate of the executed predicate instruction;

dispatching the consumer instruction to an execution unit; and

executing the consumer instruction.

4. The method of Claim 1, further comprising updating a resolved status of the predicated instruction after the predicate is resolved.

5. The method of Claim 4, wherein the resolved status of the predicated

instruction is updated in a scoreboard.

6. The method of Claim 4, further comprising:

dispatching a consumer instruction after the predicate of the predicated instruction is resolved; and

executing the consumer instruction.

7. The method of Claim 6, further comprising.

storing the result of the predicated instruction in a register, if the predicate is true; and

deleting the result of the predicated instruction in a register, if the predicate is not true.

8. A method of processing a predicated instruction comprising:

receiving a predicated instruction in an execution stage of an in-order pipeline;

stalling the predicated instruction until predicate is resolved;

storing the result of the predicated instruction in a register, if the predicate is true; and

deleting the result of the predicated instruction, if the predicate is not true.

9. The method of Claim 8, further comprising:

determining if a predicated instruction is followed by a consumer instruction in the next clock cycle, wherein the consumer instruction depends on a result of the predicated instruction; and

slipping the predicated instruction to a previous stage in the pipeline if the

predicated instruction is not followed by the consumer instruction in the next clock cycle.

10. The method of claim 9, wherein the predicated instruction is followed by a consumer instruction in the next clock cycle further comprising:

storing the predicated instruction in an associative buffer;

resolving the predicate; and

executing the consumer instruction.

11. A computer system comprising:

a processor, wherein the processor includes:

a plurality of dynamic pipeline stages including at least one predicated instruction;

a register renaming unit;

a reorder buffer;

a plurality of execution units; and

a plurality of reservation stations wherein the register renaming unit, the reorder buffer, the plurality of execution units and the plurality of reservation stations are coupled to at least one of the plurality of dynamic pipeline stages, wherein:

the predicated instruction is received in at least one of the plurality of reservation stations;

the predicated instruction is dispatched to the execution unit;

the predicated instruction is executed in the execution unit; and

a result of the executed, predicated instruction is stored in the

re-order buffer;

a system bus;

a computer memory system; and

an input/output device, wherein the system bus is coupled to the processor, the computer memory system and the input/output device.

12. The system of Claim 11, further comprising a scoreboard.

13. The system of Claim 11, wherein, after the result of the executed, predicated instruction is stored in the re-order buffer, the predicate of the executed predicate instruction is resolved and a consumer instruction is dispatched to the execution unit; and the consumer instruction is executed.

14. A computer system comprising:

a processor, wherein the processor includes:

a plurality of in-order pipeline stages including at least one predicated instruction and a consumer instruction and wherein:

the predicated instruction is received in an execution stage of the pipeline;

if the predicated instruction is not followed by the consumer instruction in the next clock cycle then the predicated instruction is slipped to a previous stage in the pipeline;

if the predicated instruction is followed by the consumer instruction in the next clock cycle then

stalling the predicated instruction until predicate is

resolved; and

storing the result of the predicated instruction in a register, if the predicate is true; and

deleting the result of the predicated instruction, if the predicate is not true.

a system bus;

a computer memory system; and

an input/output device, wherein the system bus is coupled to the processor, the computer memory system and the input/output device.

15. The system of Claim 14, wherein the memory system includes an associative buffer coupled to the pipeline.

16. The system of Claim 15, storing a predicated instruction in the associative buffer until a consumer instruction occurs in the next in clock cycle.